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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,910	07/21/2008	Sei Yang Yang	043946-4	3398

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EXAMINER

CHAD, ANISS

ART UNIT	PAPER NUMBER
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2123

NOTIFICATION DATE	DELIVERY MODE
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03/12/2010

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/591,910	Applicant(s) YANG, SEI YANG	
	Examiner Aniss Chad	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 146-152 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 146-152 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 146-152 are pending in the instant application.

Claims 1-145 have been canceled and claims 146-152 have been added by an amendment filed on 12/16/2009.

Claims 146-152 stand rejected.

Claim Objections

Claims 147-148, 152 are objected to because there is insufficient antecedent basis in the following limitations:

“the values” in claim 147 line 8, claim 148 line 7, and claim 152 line 2.

“the design state” in claim 147 line 9.

“the entire simulation time” in claim 148 line 8.

“the partial simulation time” in claim 148 lines 12-13.

“said simulation input stimuli” in claim 152 line 9.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 151-152 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 151 line 4 and claim 152 lines 3-6, 9, 11, 15-

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16, 21, 23 are indefinite because it is unclear whether the phrase contained in the parenthesis is part of the claimed subject matter or not.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 146-152 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajsuman et al. (US Patent No.: US 6678645 B1) hereinafter Rajsuman.

Regarding claim 146, Rajsuman discloses a design verification method (Fig. 2, Col. 5 lines 54-56), in which one or more design bugs in a design code or in a design netlist (Col. 3, *Static timing analysis is performed on representative netlist of cores that have been synthesized with various technology libraries.*) are identified by simulation with one or more test benches (Fig. 2, S33), comprising the following steps: at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation (Col. 6, lines 38-42, *In the next step S33, the validation method verifies timings in the cores by **using simulation testbenches for core-to-core communication and SoC level critical paths.***) and one or more post-1 st simulation runs as a back- stage

simulation, wherein a necessary information is collected from the 1st simulation run when the 1 st simulation run is in progress, and said one or more post-1 st simulation runs are executed by using said collected necessary information for obtaining visibility. (Col. 9, lines 10-15, *This data is the design-simulation testbench of the core. It **contains signal values and timing information to identify instances when signal value changes from 0-to-1 or 1-to-0, i.e., event based test patterns. Thus, no translation is necessary and the data (test pattern) is directly applied to the core (silicon IC 68).***)

Regarding claim 147, Rajsuman discloses a design verification method(Fig. 2, Col. 5 lines 54-56), in which one or more design bugs in a design code or in a design net-list are identified by simulation with one or more test benches, comprising the following steps: at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation and one or more post-1st simulation runs as a back- stage simulation (Col. 6, lines 38-42, *In the next step S33, the validation method verifies timings in the cores by **using simulation testbenches for core-to-core communication and SoC level critical paths.***), wherein a necessary information is collected from the 1st simulation run when the 1st simulation run is in progress, and said one or more post-1st simulation runs are executed by using said collected necessary information for obtaining visibility, and said necessary information consists of the values on all inputs and input/outs signals in one or more design objects and the design state of said one or more design objects. (Col. 9, lines 10-15, *This data is the design-simulation testbench of the core. It **contains signal values and timing information to identify instances when***

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signal value changes from 0-to-1 or 1-to-0, i.e., event based test patterns. Thus, no translation is necessary and the data (test pattern) is directly applied to the core (silicon IC 68).)

Regarding claim 148, Rajsuman discloses a design verification method (Fig. 2, Col. 5 lines 54-56), in which one or more design bugs in a design code or in a design net-list are identified by simulation with one or more test benches, comprising the following steps: at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation and one or more post-1 st simulation runs as a back-stage simulation (Col. 6, lines 38-42, *In the next step S33, the validation method verifies timings in the cores by using simulation testbenches for core-to-core communication and SoC level critical paths.*), wherein a necessary information is collected from a 1 st simulation run when a 1 st simulation run is in progress, said one or more post-1 st simulation runs are executed by using said collected necessary information for obtaining visibility, the values on all inputs and input/outs signals in one or more design objects are saved for the entire simulation time of said 1 st simulation run for said necessary information collected from said 1st simulation run (Col. 10, lines 13-20, *The address sequencer 88 provides address data to the event memory 90. The event memory 90 stores the timing data for each event. For example, the event memory 90 stores the event data in two separate manners, one for storing the timing data which is integer multiple of one cycle of a master (reference) clock, and the other for storing the timing data which is a fraction or fractions of one cycle of the reference clock.*) and one or

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more design states of said one or more design objects are also saved only at regular intervals in said 1st simulation run for said necessary information collected from said 1st simulation run, and said one or more post-1st simulation runs are executed only for the partial simulation time in said entire simulation time of said 1st simulation run. (Col. 7 line 60 to Col. 8, line 5, ... *application of simulation data to the silicon ICs 68.sub.1 -68.sub.5, **response comparison, scheduling of various tasks for individual blocks/cores** as well as monitoring the status of individual cores (silicon ICs) and SoC...*).

Regarding claim 149, Rajsuman discloses a design verification method (Fig. 2, Col. 5 lines 54-56), in which a simulation run at a lower level of abstraction (Col. 2, lines 16-22, *FIG. 1 illustrates the core design at different levels of abstraction and what type of verification methodology is used today at each level. From the highest to lowest abstraction levels, FIG. 1 shows behavioral HDL level 21, RTL (register transfer language) level 23, gate level 25 and physical design level 27.*) is executed by using simulation results collected (Col. 2, lines 37-40, *Regression testing which is done by running a collection of tests after any modification in the design. Each bug fix generally requires addition of a new test case with additional test conditions.*) from one or more simulation runs at a higher level of abstraction. (Fig. 1, RTL, Col. 3, lines 45-49, *For higher abstraction models, RTL models are used for the functional cores, behavioral or ISA (instruction set architecture) models for memory and processor cores and bus functional models and monitors are used to generate and check transactions with communications blocks.*)

Regarding claim 150, Rajsuman discloses a design verification method according to Claim 149 wherein: said simulation results collected from one or more simulation runs at the higher level of abstraction, which is used at a simulation run at the lower level of abstraction, contain one or more design states of the design at the higher level of abstraction, and said simulation run at the lower level of abstraction is executed in temporally parallel. (Col. 2, lines 53-55, *Another way to verify output responses is to run the actual software application, which is **basically a hardware/software co-simulation.***)

Regarding claim 151, Rajsuman discloses a design verification method (Fig. 2, Col. 5 lines 54-56) comprising: by using a verification software and at least one or more verification platforms an additional code or circuit is instrumented into a design code or into a design net-list in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that dynamic information is collected by said additional code or circuit instrumented during one or more verification runs (simulation runs or simulation acceleration runs), and the collected dynamic information is re-used at a post-debugging simulation after at least one design object is changed for debugging for reducing a total verification time. (Col. 4, lines 64-67, *It is another object of the present invention to provide a method and apparatus for SoC design validation which is capable of **performing thorough SoC design validation with high speed and low cost.***)

Regarding claim 152, Rajsuman discloses a design verification method according to Claim 151, wherein for said collected dynamic information the values on all inputs and outputs signals in one or more design objects are saved during said one or more verification runs (simulation runs or simulation acceleration runs) (Col. 9, lines 10-15, *This data is the design-simulation testbench of the core. It **contains signal values and timing information to identify instances when signal value changes** from 0-to-1 or 1-to-0, i.e., event based test patterns. Thus, no translation is necessary and the data (test pattern) is directly applied to the core (silicon IC 68).*) and one or more design states of one or more design objects are also saved only at regular intervals during said one or more verification runs (simulation runs or simulation acceleration runs) (Col. 7 line 60 to Col. 8, line 5, ... *application of simulation data to the silicon ICs 68.sub.1 -68.sub.5, **response comparison, scheduling of various tasks for individual blocks/cores** as well as monitoring the status of individual cores (silicon ICs) and SoC...*), and

after at least one design object is changed for debugging said post-debugging simulation (Col. 9, lines 28-31, ...*method and apparatus of the present invention also **allow a user to debug a fault in the core** much more easily than the present day systems...*) includes the following two simulation steps;

i) first, only said simulation input stimuli (input information for replay), and the values on its outputs are compared with that of the design object saved during said one or more verification runs (simulation runs or simulation acceleration runs) before at least one design object is changed for debugging, and during this simulation one or more design states of said design object changed for debugging are also saved only at said

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regular intervals, and this simulation stops when the values on its outputs are different from that of the design object saved during said one or more verification runs(simulation runs or simulation acceleration runs) before at least one design object is changed for debugging, (Col. 8, lines 29-34, *The driver is to **apply the test pattern to an input pin of the DUT and the comparator compares a response output of the DUT with an expected value.** The performance board is used to mechanically and electrically connect the DUT under test with the verification unit (VU) 66.*)

ii) second, both changed design object and unchanged design objects are simulated together, but, unchanged design objects are simulated not from the simulation time O, but from one of the design checkpoints made in said one or more verification runs(simulation runs or simulation acceleration runs) after restoring the design state for said unchanged design object, which had been previously saved during said one or more verification runs(simulation runs or simulation acceleration runs). (Col. 11, lines 31-36, *Once functionality of the individual cores, interface and glue logic is verified, **timing verification is checked at SoC level critical paths.** It should be noted that after completion of the steps 31 and 32 of FIG. 2, all individual pieces of SoC and interconnection are available on the design validation station of the present invention.*)

Response to Arguments

Applicant's arguments with respect to new claims 146-152 regarding the §102 rejections have been considered but they are not persuasive.

With respect to Claim 123 (New Claim 146):

Applicant argues that in Rajsuman, there is no disclosure or suggestion of any such simulation method and that Rajsuman does not mention or suggest re-using a data file in other simulation for the specific purpose of visibility. The examiner respectfully disagrees. Rajsuman teaches re-using a data file in other simulation for the specific purpose of visibility (Col. 9, lines 10-15, *This data is the design-simulation testbench of the core. It **contains signal values and timing information to identify instances (i.e. visibility) when signal value changes** from 0-to-1 or 1-to-0, i.e., event based test patterns. Thus, no translation is necessary and the data (test pattern) is directly applied to the core (silicon IC 68).*)

Applicant also argues that both the recited 1st simulation run and the post-1st simulation runs in the claimed simulation method are always carried out with the entire design under verification, i.e. the entire SoC. Hence, the simulation method in the present invention and the simulation method disclosed in Rajsuman are very different in kind from each other. The examiner respectfully disagrees. Rajsuman discloses that both the recited 1st simulation run and the post-1st simulation runs in the claimed simulation method are always carried out with the entire design under verification (Col. 3, lines 34-35, *The main goal of SoC design validation is **to verify the entire system** the way it would be used by the end user.*).

With respect to Claim 127 (New Claim 149):

Applicant argues that Rajsuman does not disclose that the simulation result of the higher level of abstraction is re-used in the simulation of the lower level of abstraction, that FIG. 1 of Rajsuman neither discloses nor suggests such a simulation method, but

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simply illustrates the core design at different levels of abstraction and what type of verification methodology is used today at each level. Hence FIG. 1 of Rajsuman does not disclose or suggest the recited back-stage simulation runs using the design at the lower level of abstraction is executed by re-using the necessary information collected from a front-stage simulation run using the design at the higher level of abstraction. The examiner respectfully disagrees. Rajsuman discloses in Col. 2, lines 16-22, *"FIG. 1 illustrates the core design at **different levels of abstraction and what type of verification methodology is used today at each level**. From the highest to lowest abstraction levels, FIG. 1 shows behavioral HDL level 21, RTL (register transfer language) level 23, gate level 25 and physical design level 27"*. Rajsuman further discloses in Col. 2, lines 37-40, *"Regression testing which is done by running a collection of tests after any modification in the design (i.e. the necessary information collected from a front-stage simulation run). Each bug fix generally requires addition of a new test case with additional test conditions"*. Finally Rajsuman discloses in Col. 3, lines 45-49, *"For higher abstraction models, RTL models are used for the functional cores, behavioral or ISA (instruction set architecture) models for memory and processor cores and bus functional models and monitors are used to generate and check transactions with communications blocks"*.

With respect to Claim 137 (New Claim 151):

Applicant argues that Rajsuman discloses only observation or data-obtaining after executing the application, not that an "additional code is instrumented into the design code." Applicant also argues that Rajsuman does not disclose that a data file generated

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before the design is modified could be re-used in post-debugging simulation for faster post-debugging simulation. The examiner respectfully disagrees. See above response to argument regarding claim 149. In addition, Rajsuman teaches “the collected dynamic information is re-used at a post-debugging simulation after at least one design object is changed for debugging for reducing a total verification time” (Col. 4, lines 64-67, *It is another object of the present invention to provide a method and apparatus for SoC design validation which is capable of performing thorough SoC design validation with high speed and low cost.*).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aniss Chad whose telephone number is (571)270-3832. The examiner can normally be reached on M-F 9-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571)272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aniss Chad/
Examiner, Art Unit 2123

/Paul L Rodriguez/

Supervisory Patent Examiner, Art Unit 2123